

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Susie Xiuru YANG et al.

Serial No. 10/809,908

Filed: March 26, 2004

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: Group Art Unit:  
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: Examiner:

For: IMPROVED CONTROL OF METAL RESISTANCE IN SEMICONDUCTOR  
PRODUCTS VIA INTEGRATED METROLOGY

**INFORMATION DISCLOSURE STATEMENT**

Honorable Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom. Copies of any cited U.S. Patents and U.S. Patent Publications are not being submitted in accordance with 37 CFR 1.98(a)(2)(i).

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

In accordance with 37 C.F.R. § 1.97(g) and (h), the filing of this IDS should not be construed as a representation that a search had been made or that information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56 (b), or that any cited document listed or attached is (or constitutes) prior art. Unless otherwise indicated, the date of

publication indicated for an item is taken from the face of the item, and Applicant reserves the right to prove that the date of publication is in fact different.

The references listed on Sheet 1 of the attached PTO-1449 Forms were cited in a patentability investigation and/or a corresponding foreign or PCT application relating to the above-referenced application. The remaining references are from potentially related patent applications, and possibly other sources.

No fee is believed to be required; however, the Commissioner is authorized to charge any deficiency in any fees pursuant to 37 CFR § 1.17 associated with this communication and to credit any excess payment to Deposit Account No. 08-0219.

Respectfully submitted,

WILMER CUTLER PICKERING HALE AND DORR LLP

A handwritten signature in black ink, appearing to read "SMA Alter", is written over the printed name.

Scott M. Alter

Registration No. 32,879

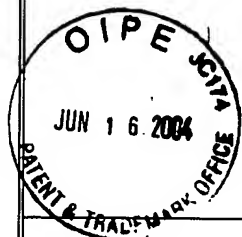
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Date: 6/16/04

**INFORMATION DISCLOSURE  
CITATION IN AN  
APPLICATION  
(PTO-1449)**



ATTY. DOCKET NO.  
008066 USA/PMG/PCTRL

SERIAL NO.  
10/809,908

APPLICANT  
Susie Xiuru YANG et al.

FILING DATE  
March 26, 2004

GROUP

**U.S. PATENT DOCUMENTS**

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EXAMINER

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				APPLICANT Susie Xiuru YANG et al.			
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EXAMINER'S INITIALS	PATENT APP. NO.	FILING DATE	NAME	TITLE	CLASS	SUB- CLASS	
	09/363,966	07/29/99	Arackaparambil et al.	Computer Integrated Manufacturing Techniques			
	09/469,227	12/22/99	Somekh et al.	Multi-Tool Control System, Method and Medium			
	09/619,044	07/19/00	Yuan	System and Method of Exporting or Importing Object Data in a Manufacturing Execution System			
	09/637,620	08/11/00	Chi et al.	Generic Interface Builder			
	09/656,031	09/06/00	Chi et al.	Dispatching Component for Associating Manufacturing Facility Service Requestors with Service Providers			
	09/655,542	09/06/00	Yuan	System, Method and Medium for Defining Palettes to Transform an Application Program Interface for a Service			
	09/725,908	11/30/00	Chi et al.	Dynamic Subject Information Generation in Message Services of Distributed Object Systems			
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<b>EXAMINER'S INITIALS</b>	<b>PATENT APP. NO.</b>	<b>FILING DATE</b>	<b>NAME</b>	<b>TITLE</b>	<b>CLASS</b>	<b>SUB- CLASS</b>			
	10/084,092	02/28/02	Arackaparambil et al.	Computer Integrated Manufacturing Techniques					
	10/100,184	03/19/02	Al-Bayati et al.	Method, System and Medium for Controlling Semiconductor Wafer Processes Using Critical Dimension Measurements					
	10/135,405	05/01/02	Reiss et al.	Integration of Fault Detection with Run-to-Run Control					
	10/135,451	05/01/02	Shanmugasundram et al.	Dynamic Metrology Schemes and Sampling Schemes for Advanced Process Control in Semiconductor Processing					
	10/172,977	06/18/02	Shanmugasundram et al.	Method, System and Medium for Process Control for the Matching of Tools, Chambers and/or Other Semiconductor-Related Entities					
	10/173,108	06/18/02	Shanmugasundram et al.	Integrating Tool, Module, and Fab Level Control					
	10/174,370	06/18/02	Shanmugasundram et al.	Feedback Control of Plasma-Enhanced Chemical Vapor Deposition Processes					
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	10/632,107	08/01/03	Schwarm et al.	Method, System, and Medium for Handling Misrepresentative Metrology Data Within an Advanced Process Control System					
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	10/759,108	01/20/04	Schwarm	Automated Design and Execution of Experiments with Integrated Model Creation for Semiconductor Manufacturing Tools					
	10/765,921	01/29/04	Schwarm	System, Method, and Medium for Monitoring Performance of an Advanced Process Control System					
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	10/809,906	03/26/04	Surana et al.	A Technique for Process-Qualifying a Semiconductor Manufacturing Tool Using Metrology Data			
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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation			
						Yes	No		
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	61-171147	08/01/86	Japan			X			
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	2,050,247	08/29/91	Canada			X			
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	3-202710	09/04/91	Japan			X			
	05-151231	06/18/93	Japan			X			
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	05-266029	10/15/93	Japan			X			
	06-110894	04/22/94	Japan			X			
	06-176994	06/24/94	Japan			X			
	06-184434	07/05/94	Japan			X			
	06-252236	09/09/94	Japan			X			
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	EP 0 621 522 A2	10/26/94	Europe			X			
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						Yes	No
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	EP 0 877 308 A2	11/11/98	Europe			X	
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		<b>FILING DATE</b> March 26, 2004	<b>GROUP</b>
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<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)</b>	ATTY. DOCKET NO. 008066 USA/PMG/PCTRL	SERIAL NO. 10/809,908
	APPLICANT Susie Xiuru YANG et al.	
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		<b>APPLICANT</b> Susie Xiuru YANG et al.	
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